Power Efficient Full Adder using Adiabatic Logic

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Abstract—*In this paper power dissipation of a fully adiabatic logic circuit has been showed, which is compared with its static CMOS and 2PASCL. This paper proposed a new design of true single phase adiabatic circuitry (TSEL) and static energy recovery full (SERF) adder. The simulation is done in NI-MULTISIM software at 0.18 µm and 1.5 µm, 3V CMOS standard process technology with a frequency range of 200-800MHz.This results shows the importance of adiabatic logic in the modern digital field.*

1. INTRODUCTION

In this modern technology, power consumption is one of the main concerns. Normally power effects on the system cost, that's why power dissipation should be less as much as possible. All electronic devices which are portable, versatile and it gives low power. The current static CMOS technology gives the basis for low power dissipation with an advantage of small fabrication space compared to similar technologies. This kind of power dissipation is dynamic in nature and that is why adiabatic logic is a good approach to reduce dynamic power dissipation [1] [2] [3] [4] [5].

This paper includes one of the logic families of adiabatic logic that is true single phase adiabatic circuitry (TSEL) and static energy recovery full (SERF) adder. These circuits are first designed and simulated in MULTISIM software and finally a power dissipation comparison table of adiabatic array logic [1] along with static CMOS and 2PASCL based is shown.

Adiabatic logic helps in handling with the power dissipation problem. For output evaluation of a circuit, it follows a totally different approach .In adiabatic approach, conventional static CMOS by replacing its DC power supply by a sinusoidal power source, called the power clock [2].

1.1 A review of power dissipation

While using the CMOS circuit, amount of power consumed can be decomposed in two groups: static and dynamic.

1.1.1 Static power

Static power is also called steady state power. And static power dissipation of a circuit is given by the relation:

$$P_{stat} = I_{stat} V_{DD} \quad \ldots\ldots\ldots\ldots \quad (1)$$

When there is no switching activity, I_{stat} is the amount of current flowing through the circuit. There is no direct path from V_{DD} to ground as PMOS and NMOS transistors [8], which cannot turn on simultaneously; hence CMOS circuits dissipate no static (DC) power in the steady state.

1.1.2 Dynamic power

From the transient switching action of the CMOS device, dynamic component of power dissipation appears [3]. It can be further divided in two groups Switching Power, Short circuit Power and leakage current [4].

While switching transient, at some point both the NMOS and PMOS devices will be turned on. This occurs for the gate voltages between V_{tn} and $V_{DD} - V_{tp}$ .sThe dynamic or switching power dissipation of a circuit is expressed by the following relation:

$$P_{dyn} = \alpha C V^2_{DD} f \quad \ldots\ldots \quad (2)$$

Here, α is the switching activity, it goes from 0 to 1 for every transition, V_{DD} is the power supplied to the circuit, C is the load capacitance, and f is clock frequency [11].

2. ADIABATIC LOGIC

Now the question is from where "adiabatic" term comes, this term comes from thermodynamics. According to this process, there is no exchange of heat with the environment. Adiabatic logic gates operation consists of two stages, one for evaluation of logic and another for resetting the gate output logic value.

3. THE CHARGING PROCESS IN ADIABATIC LOGIC COMPARED TO STATIC LOGIC

Fig. 1 depicts the amount of dissipated energy of a simple CMOS inverter. Either the PMOS device or the NMOS device is on, it only depends on the input signal the remainder is off. Energy can be moved from the voltage sources for the charging of the capacitor at the output to the voltage source V_{DD}, when input transition occurs from 1 to 0. Amount of

stored charge of $Q=CV_{DD}$ is coming from the source of voltage.

$$E_{V_{DD}} = QV_{DD} = CV_{DD}^{2} \quad \ldots\ldots\ldots \quad (3)\ [7]$$

Amount of stored energy on the capacitor on voltage V_{DD} is given by

$$E_C = \frac{1}{2} CV_{DD}^{2} \quad \ldots\ldots\ldots \quad (4)$$

From the above two equations, the variance between the given energy and the stored energy dissipated in the PMOS switch is shown.

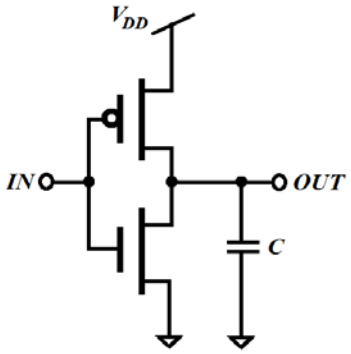

Fig. 1: A static CMOS inverter

In the charging process of adiabatic logic there are four intervals- evaluate (E), hold (H), recover (R) and wait (W), as depicted in fig. 2 [15].

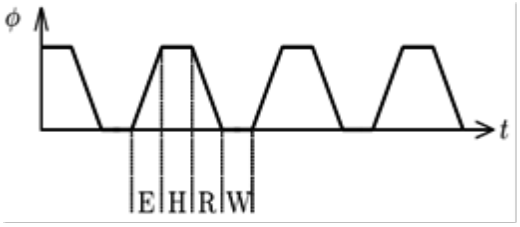

Fig. 2: Phases in an Adiabatic Power Supply

In the interval of evaluate, the outputs are preserved so as to be applied to the successive circuits, during the hold interval. Then, in the recover interval, energy is retrieved and move back to the power supply which is the main purpose of employing adiabatic logic. Finally, to evade inequality, a wait interval is showed.

4. ADIABATIC ARRAY LOGIC

The adiabatic array logic composed of an array of transmission gates to design an AND-plane and a wired OR plane forms the second plane. Depend on array logic [10], the circuit drives a sinusoidal power supply, the power clock. This logic is presented in fig.3 [4]. AAL is used to implement circuits which basically have BOOLEAN terms based expressions.

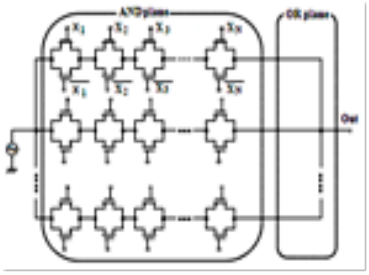

Fig. 3: Adiabatic Array Logic

5. CIRCUIT DESIGN OF TRUE SINGLE PHASE ADIABATIC CIRCUITRY (TSEL) AND SIMULATION

This paper includes true single-phase adiabatic circuit family which can be used for speedy and low-energy VLSI design. The circuit is designed and simulated in MULTISIM with a variation of arithmetic circuits and with 0.5m standard CMOS process parameters, 200MHZ-800MHZ ranging frequencies and with a power clock of 3V.

5.1 True single phase adiabatic circuitry (TSEL)

TSEL is one of the simplest members of the family. Here a single-phase sinusoidal power-clock power is given to TSEL gates. TSEL is nothing but combination of alternating PMOS and NMOS gates. For providing speedy and high-capability operation, it requires two dc reference voltages. This section described the design and function of TSEL.

5.2 Gates of TSEL

The basic design of a TSEL PMOS gate PMOS inverter of includes a Combination of cross-coupled transistors MP1 and MP2, a combination of current control switches MP3 and MP4, and lastly it contains two function blocks MP5and MP6 [12]. The port gives the sinusoidal power-clock and PMOS gate is given a constant reference voltage by the port. TSEL is different from the other family by the current control switches and the reference voltages which are the primary condition.

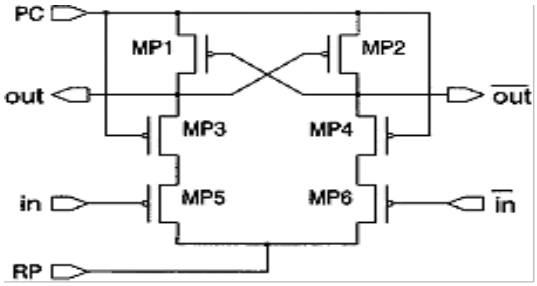

Fig. 4: A PMOS inverter in TSEL.

5.3 Circuit diagram

The circuit design of TSEL adiabatic logic is given below:

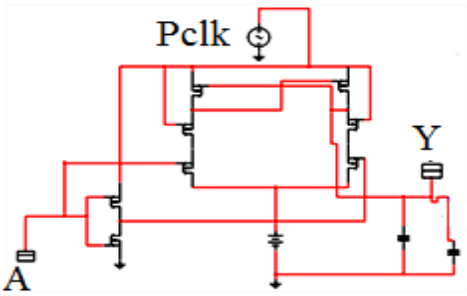

Fig. 5: Proposed TSEL inverter circuit

5.4 Simulated waveforms

Upon simulation, the output waveforms were obtained as shown below:

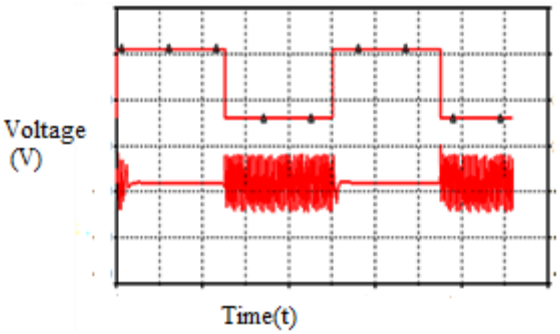

Fig. 6: Proposed TSEL input output waveforms

5.5 Power plot

Here power plot comparison are shown in NI-MULTISIM software at 0.18 µm, 3V CMOS standard process technology with W/L= 0.6 µm/0.18 µm for both PMos and NMos, $V_{PCLK} = 3V$ (peak-to-peak) and load capacitance $0.10pF$, are simulated and the following power plot was obtained. The power plot for the power dissipation curves of the different logic styles are given in figure.

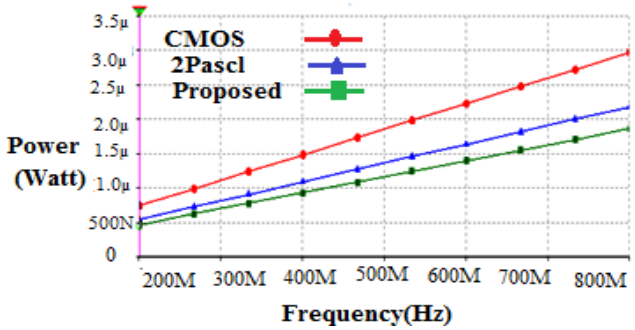

Fig. 7: Power plot comparison of TSEL

5.6 Power dissipation analysis tables

The given below table compares the performance of the TSEL at two different frequencies , 200 MHZ and 250 MHZ for the terms of transistor count, area per chip and most important the power dissipation.

Table 1: Performance analysis of various logic styles for TSEL

LOGIC PARAMETER		STATIC	2PASCL	AAL
TRANSISTOR COUNT		8	16	8
AREA PER CHIP (μm^2)		0. 864	1.728	0. 864
TOTAL POWER DISSIPATION (nW)	AT 200 MHZ	742.688	544.670	465.261
	AT 250 MHZ	928.359	680.837	581.577

Table 2: Percentage power saving of proposed logic with respect to standard logic styles for TSEL

2PASCL	STATIC
14.57%	37.35%

***NOTE*:** Area per chip=W*L*Transistor count

6. CIRCUIT DESIGN OF STATIC ENERGY RECOVERY FULL (SERF) ADDER AND SIMULATION

This paper introduces static energy recovery full (SERF) adder [6]. It requires only 10 transistors instead of 28 transistors. In the 10T adder or SERF adder cell, using pass transistor logic implementation of XOR and XNOR of A and B is done and one inverter is there which is used to complement the input signal A [13] [14] . We have showed the circuits for static SERF, adiabatic SERF and 2Pascl SERF. SERF itself consumes less power, even using adiabatic logic it gives less power than the static circuit.

6.1 Implementation of adder

For the implementation of adder, there will be needed a 1-bit full adder which consists of three bit inputs (A, B, and C) and also two 1-bit outputs (sum and carry). Now the correlation between the inputs and outputs are given below

$$SUM=\overline{A}\,\overline{B}C+\overline{A}B\overline{C}+A\overline{B}\,\overline{C}+ABC$$

$$CARRY=AB+BC+CA$$

6.2 Circuit diagram

The circuit design of SERF adiabatic logic is given below:

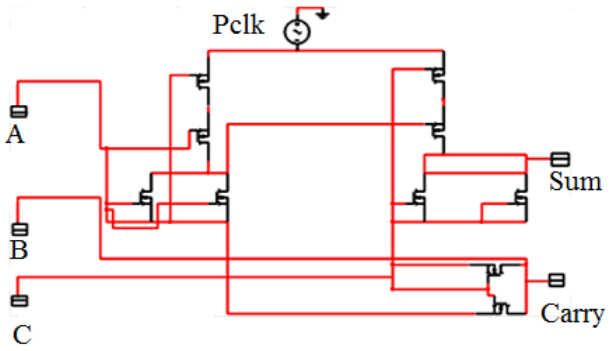

Fig. 8: Proposed AAL SERF adder

6.3 Simulated waveforms:

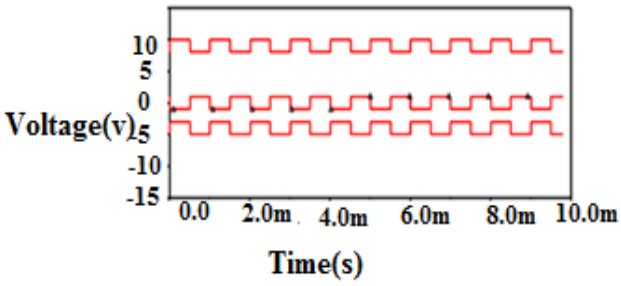

Fig. 9: Proposed SERF adder inputs

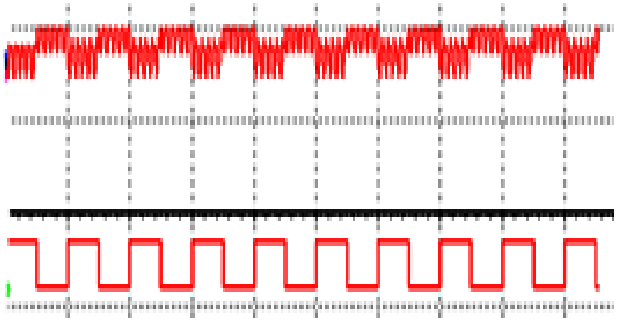

Fig. 10: Proposed SERF adder output

6.4 Power plot

Here power plot comparison are shown in NI-MULTISIM software at 1.5 µm, 3V CMOS standard process technology with W/L= 0.75 µm/1.5 µm for both PMos and NMos, $V_{PCLK} = 3V$ (peak-to-peak), are simulated and the following power plot was obtained. The power plot featuring the power dissipation curves of the different logic styles are given in figure.

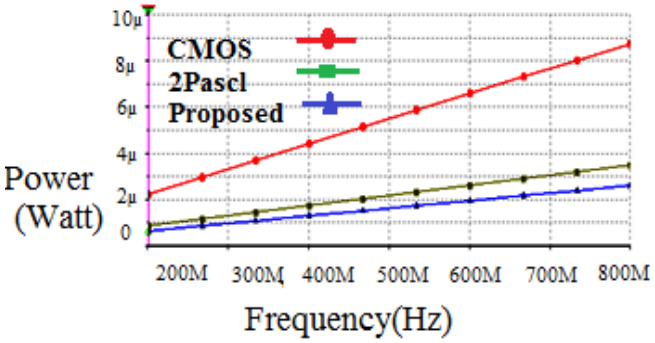

Fig. 11: Power plot comparison of SERF

6.5 Power dissipation analysis tables:

The given below table compares the performance of the SERF at two different frequencies ,200 MHZ and 250 MHZ in terms of transistor count, area per chip and most important the power dissipation.

Table 3: Performance analysis of various logic styles for SERF

LOGIC PARAMETER		STATIC	2PASCL	AAL
TRANSISTOR COUNT		10	20	10
AREA PER CHIP (μm^2)		11.25	22.5	11.25
TOTAL POWER DISSIPATION	AT 200 MHZ	2.212 µ	867.8697 n	650.903 n
	AT 250 MHZ	2.760 µ	1.0848 µ	813.628 n

Table 4: Percentage power saving of proposed logic with respect to standard logic styles for SERF

2PASCL	STATIC
24.99%	70.03%

7. CONCLUSIONS

The primary aim was to present the power dissipation of true single phase adiabatic circuitry (TSEL) and static energy recovery full (SERF) adder using Static CMOS Logic, adiabatic logic array, Two Phase Clocked Adiabatic and (2PASCL) which was successfully designed and implemented. There is tremendous amount of power saving in both the circuits by using adiabatic logic array and successfully implement the design.

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